Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A method for forming a self-aligned low temperature polysilicon thin film transistor (LTPS TFT), the method comprising the steps of:

providing a substrate comprising an N type LTPS TFT region and a P type LTPS TFT region;

sequentially forming a patterned undoped polysilicon layer, a dielectric layer, and a patterned conductive layer, the patterned conductive layer comprising two first gaps;

performing a first implantation process to implant N type dopants via the first gaps into the undoped patterned polysilicon layer to form a source and a drain;

removing a certain width of the patterned conductive layer to form two second gaps and to define a gate of an N type LTPS TFT;

performing a second implantation process to implant N type dopants via the second gaps into the undoped patterned polysilicon layer to form two lightly doped drains;

forming a gate of a P type LTPS TFT in the P type LTPS TFT region; and

forming a source and a drain of the P type LTPS TFT in the P type LTPS TFT region.

[c2] 2.The method of claim 1 wherein the substrate is a glass substrate or a quartz substrate.

[c3] 3.The method of claim 1 wherein a buffer layer exists between the substrate and the patterned undoped polysilicon layer.

[c4] 4.The method of claim 1 wherein the step of forming the patterned undoped polysilicon layer further comprises:
performing a sputtering process to form an amorphous silicon (α-Si) layer on the substrate;
performing an annealing process, such that the amorphous silicon layer is recrystallized and turned a polysilicon layer; and
performing a photo-etching process (PEP) to form a patterned undoped polysilicon layer in each polysilicon layer of the N type LTPS TFT region and the P type LTPS TFT region.

[c5] 5.The method of claim 1 wherein the material of the dielectric layer comprises silicon oxide or silicon nitride.

[c6] 6.The method of claim 1 wherein the step of forming the two first gaps and the two second gaps further comprises:
forming a first conductive layer and a first patterned photo resist layer on the dielectric layer;

removing the conductive layer that is not covered by the first patterned photo resist layer to form the two first gaps in the conductive layer of the N type LTPS TFT region;

performing a trimming process to reduce a certain width of the first patterned photo resist;

removing the conductive layer that is not covered by the reduced first patterned photo resist layer, such that the two second gaps are formed in the conductive layer of the N type LTPS TFT region; and

removing the reduced first patterned photo resist layer.

[c7] 7.The method of claim 6 wherein the width of each first gap is smaller than the width of each second gap.

[c8] 8.The method of claim 6 wherein the material of the conductive layer is selected from the group consisting of aluminum, wolfram, chromium, and molybdenum.

[c9] 9.The method of claim 6 wherein the trimming process comprises an ash process, a descum process, and an ultraviolet beaming process or a thermal curing process.

[c10] 10.The method of claim 1 wherein the dopant concentration in the first implantation process is about 1E14 to 1E16 atoms/cm^2, and the N type dopants comprise arsenic or phosphorous.

[c11] 11.The method of claim 1 wherein the dopant concentration in the second implantation process is about 1E12 to 1E14 atoms/cm^2, and the N type dopants comprise arsenic or phosphorous.

[c12] 12.The method of claim 1 wherein the step of forming the gate of the P type LTPS TFT further comprises:
forming a second patterned photo resist layer to cover the gate of the N type LTPS TFT and parts of the P type LTPS TFT region for defining the gate of the P type LTPS TFT;
removing the patterned conductive layer that is not covered by the second patterned photo resist layer, such that the gate of the P type LTPS TFT is formed; and
removing the second patterned photo resist layer.

[c13] 13.The method of claim 12 wherein the step of forming the source and the drain further comprises:
forming a third patterned photo resist layer, the third patterned photo resist layer covering the gate of the P type LTPS TFT;
performing a third implantation process to implant P type dopants to form the source and the drain of the P type LTPS TFT; and
removing the third patterned photo resist layer.

[c14] 14.The method of claim 13 wherein the dopant concentration in the third implantation is about 1E14 to 1E16 atoms/cm^2, and the P type dopants comprise boron or boron fluoride (BF_2).

[c15] 15.The method of claim 1 wherein the step of forming the gate, the source, and the drain of the P type LTPS TFT further comprises:
forming a fourth patterned photo resist layer, the fourth photo resist layer covering the gate of the P type LTPS TFT;
removing the patterned conductive layer that is not covered by the fourth patterned photo resist layer, such that the gate of the P type LTPS TFT is formed.

[c16] performing a fourth implantation process to form the source and the drain of the P type LTPS TFT;
removing the fourth patterned photo resist layer;
forming a fifth patterned photo resist layer to cover the gate of the N type LTPS TFT and the gate of the P type LTPS TFT;
removing the patterned conductive layer that is not covered by the fifth patterned photo resist layer; and
removing the fifth patterned photo resist layer.

[c17] 16.The method of claim 1 wherein the N type LTPS TFT is installed in a pixel array area of the substrate as a

switching device of a pixel cell of an LCD.

[c18] 17.The method of claim 16 wherein the P type LTPS TFT and the N type LTPS TFT are low temperature polysilicon complementary metal-oxide-semiconductor thin film transistors (LTPS CMOS TFTs), and are installed in a periphery circuit area of the LCD as a logic device of the periphery circuit of the LCD.

[c19] 18.A method for forming a self-aligned low temperature polysilicon thin film transistor (LTPS TFT), the method comprising the steps of:
providing a substrate comprising an N type LTPS TFT region and a P type LTPS TFT region;
sequentially forming a patterned undoped polysilicon layer, a dielectric layer, a conductive layer, and a first patterned photo resist layer, the first patterned photo resist layer comprising two first gaps;
performing an isotropic etching process to remove parts of the conductive layer via the two first gaps to form two second gaps, and to form a gate of an N type LTPS TFT;
implanting N type dopants into the patterned undoped polysilicon layer of the N type LTPS TFT region to form a source and a drain of the N type LTPS TFT;
removing the first patterned photo resist layer;
implanting N type dopants into the patterned undoped polysilicon layer of the N type LTPS TFT region to form

two lightly doped drains (LDD) of the N type LTPS TFT;
forming a gate of a P type LTPS TFT in the P type LTPS TFT region; and
forming a source and a drain of the P type LTPS TFT in the P type LTPS TFT region.

[c20] 19.The method of claim 18 wherein the substrate is a glass substrate of a quartz substrate.

[c21] 20.The method of claim 18 wherein a buffer layer exists between the substrate and the patterned undoped polysilicon layer.

[c22] 21.The method of claim 18 wherein the step of forming the patterned undoped polysilicon layer further comprises:
performing a sputtering process to form an amorphous silicon (α-Si) layer on the substrate;
performing an annealing process, such that the amorphous silicon layer is recrystallized and turned a polysilicon layer; and
performing a photo-etching process (PEP) to form a patterned undoped polysilicon layer in both the N type LTPS TFT region and the P type LTPS TFT region.

[c23] 22.The method of claim 18 wherein the material of the dielectric layer comprises silicon oxide or silicon nitride.

[c24] 23.The method of claim 18 wherein the width of each first gap of the first patterned photo resist layer is smaller than the width of each second gap.

[c25] 24.The method of claim 18 wherein the material of the conductive layer is selected from the group consisting of aluminum, wolfram, chromium, and molybdenum.

[c26] 25.The method of claim 18 wherein the N type dopants comprise arsenic or phosphorous.

[c27] 26.The method of claim 18 wherein the P type dopants comprise boron or boron fluoride (BF_2).

[c28] 27.The method of claim 18 wherein the step of forming the gate of the P type LTPS TFT further comprises:
forming a first patterned photo resist layer to cover the gate of the N type LTPS TFT and parts of the P type LTPS TFT region for defining the gate of the P type LTPS TFT;
removing the conductive layer that is not covered by the first patterned photo resist layer, such that the gate of the P type LTPS TFT is formed; and
removing the first patterned photo resist layer.

[c29] 28.The method of claim 18 wherein the step of forming the source and the drain further comprises:
forming a second patterned photo resist layer on the

substrate;

implanting P dopants into the patterned undoped polysilicon layer of the P type LTPS TFT region by utilizing the second patterned photo resist layer and the gate of the P type LTPS TFT as a mask, such that the source and the drain of the P type LTPS TFT are formed; and

removing the second patterned photo resist layer.

[c30] 29.The method of claim 18 wherein the step of forming the gate, the source, and the drain of the P type LTPS TFT further comprises:

forming a third patterned photo resist layer, the third photo resist layer exposing parts of the patterned undoped polysilicon layer of the P type LTPS TFT region;

removing the patterned conductive layer that is not covered by the third patterned photo resist layer to form the gate of the P type LTPS TFT;

implanting P dopants into the patterned undoped polysilicon layer of the P type LTPS TFT region by utilizing the gate of the P type LTPS TFT and the third patterned photo resist layer as a mask, such that the P type source and the drain of the P type LTPS TFT are formed;

removing the third patterned photo resist layer;

forming a fourth patterned photo resist layer to cover the gate of the N type LTPS TFT and the gate of the P type LTPS TFT;

removing the patterned conductive layer that is not covered by the fourth patterned photo resist layer; and removing the fourth patterned photo resist layer.

[c31] 30.The method of claim 18 wherein the N type LTPS TFT is installed in a pixel array area as a switching device of a pixel cell of an LCD.

[c32] 31.The method of claim 30 wherein the P type LTPS TFT and the N type LTPS TFT are low temperature polysilicon complementary metal-oxide-semiconductor thin film transistors (LTPS CMOS TFTs), and are installed in a periphery circuit area of the LCD as a logic device of the periphery circuit of the LCD.

[c33] 32.The method of claim 18 wherein the isotropic etching process is a wet etching process.